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EXAMINER
MANDALA, VICTOR A

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/062,714	Applicant(s) KER ET AL.
	Examiner Victor A Mandala Jr.	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-17 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication 2002/0084490 Ker et al., (The English translation of Taiwanese Patent No. 90100080), in view of U.S. Patent No. 5,824,573 Zhang et al.

1. Referring to claim 1, an integrated circuit device, comprising: a semiconductor substrate, (Zhang et al. Figure 2D #101); an isolation layer, (Zhang et al. Figure 2 D #102), formed over the semiconductor substrate, (Zhang et al. Figure 2D #101); and a layer of silicon material, (Zhang et al. Figure 2D #111-116), formed over the isolation layer, (Zhang et al. Figure 2D #102), including a first p-type portion, (Ker et al. Figure 9 #44 & Zhang et al. Figure 2D #116), a first n-type portion, (Ker et al. Figure 9 #46b & Zhang et al. Figure 2D #115), contiguous with the first p-type portion, (Ker et al. Figure 9 #44 & Zhang et al. Figure 2D #116), a second p-type portion, (Ker et al. Figure 9 #52 & Zhang et al. Figure 2D #114), contiguous with the first n-type portion, (Ker et al. Figure 9 #46b & Zhang et al. Figure 2D #115), a second n-type portion, (Ker et al. Figure 7 #42 & Zhang et al. Figure 2D #113), contiguous with the second p-type portion,

(Ker et al. Figure 9 #52 & Zhang et al. Figure 2D #114), a third p-type portion, (Ker et al. Figure 7 #46b & Zhang et al. Figure 2D #112), contiguous with the second n-type portion, (Ker et al. Figure 7 #42 & Zhang et al. Figure 2D #113), and a third n-type portion, (Ker et al. Figure 7 #46 & Zhang et al. Figure 2D #111), contiguous with the third p-type portion, (Ker et al. Figure 7 #46b & Zhang et al. Figure 2D #112), wherein the first, second, and third p-type portions and the first, second, and third n-type portions collectively form a rectifier, (Ker et al. (PMOS) Figure 7 #46, 44b, 42, & 44a & (NMOS) Figure 9 #44, 46b, 46a, 52 and Zhang et al. Figure 2D #111-116), wherein the first p-type portion, (Ker et al. (PMOS) Figure 7 #44b and Zhang et al. Figure 2D #116), and the first n-type portion, (Ker et al. (PMOS) Figure 7 #46 and Zhang et al. Figure 2D #115), form a cathode of the rectifier, and wherein the third n-type portion, (Ker et al. (NMOS) Figure 9 #46b and Zhang et al. Figure 2D #111), and the third p-type portion, (Ker et al. (NMOS) Figure 9 #44 and Zhang et al. Figure 2D #112), form an anode of the rectifier. Ker et al. teaches all of the claimed matter in claim 1 except for the rectifier consisting of a CMOS circuit in a detailed Figure but instead teaches it as separate NMOS and PMOS circuitry. Ker et al. does teach the benefits of a CMOS ESD protection circuit in Paragraph 0004. Zhang et al. does teach a CMOS circuit with the source and drain regions of the NMOS and PMOS transistors in a contiguous layout. It would have been obvious to one skilled in the art to combine the teachings of Ker et al. with the teachings of Zhang et al. because the having the source and the drain region contiguously connected reduces the off current and allows the device to be made smaller.

2. Referring to claim 2, an integrated circuit device, wherein the second p-type portion, (Ker et al. Figure 9 #52), is contiguous with the first p-type portion, (Ker et al. Figure 9 #44).

3. Referring to claim 3, an integrated circuit device, wherein the third n-type portion, (Ker et al. Figure 7 #46), is contiguous with the second n-type portion, (Ker et al. Figure 7 #42).

4. Referring to claim 4, an integrated circuit device, wherein the second p-type portion, (Ker et al. Figure 9 #52), includes the first n-type portion, (Ker et al. Figure 9 #46b), and the first p-type portion, (Ker et al. Figure 9 #44), each of which being spaced apart from the isolation layer, (Zhang et al. Figure 2 D #102).

5. Referring to claim 5, an integrated circuit device, wherein the second p-type portion, (Ker et al. Figure 9 #52), additionally includes a fourth n-type portion, (Ker et al. Figure 9 #46a), spaced apart from the first n-type portion, (Ker et al. Figure 9 #46b), the first n-type portion, (Ker et al. Figure 9 #46b), and the fourth n-type portion, (Ker et al. Figure 9 #46a), defining a source region and a drain region of an NMOS transistor.

6. Referring to claim 6, an integrated circuit device, wherein the second n-type portion, (Ker et al. Figure 7 #42), includes the third n-type portion, (Ker et al. Figure 7 #46), and the third p-type portion, (Ker et al. Figure 7 #46b), each of which being spaced apart from the isolation layer, (Zhang et al. Figure 2 D #102).

7. Referring to claim 7, an integrated circuit device, wherein the second n-type portion, (Ker et al. Figure 7 #42), additionally comprises a fourth p-type portion, (Ker et al. Figure 7 #44b), spaced apart from the third p-type portion, (Ker et al. Figure 7 #46b), the third p-type portion, (Ker et al. Figure 7 #46b), and the fourth p-type portion, (Ker et al. Figure 7 #44b), defining a source region and a drain region of a PMOS transistor.

8. Referring to claim 8, an integrated circuit device, wherein the first n-type portion, (Ker et al. Figure 9 #46b & Zhang et al. Figure 2D #115), and the first p-type portion, (Ker et al. Figure

9 #44 & Zhang et al. Figure 2D #116), are contiguous with the isolation layer, (Zhang et al. Figure 2 D #102).

9. Referring to claim 9, an integrated circuit device, wherein the second p-type portion, (Ker et al. Figure 9 #52), includes a fourth n-type portion, (Ker et al. Figure 9 #46a), formed spaced apart from the first n-type portion, (Ker et al. Figure 9 #46b), and wherein the first n-type portion, (Ker et al. Figure 9 #46b), and the fourth n-type portion, (Ker et al. Figure 9 #46a), define a source region and a drain region of an NMOS transistor.

10. Referring to claim 10, an integrated circuit device, wherein the NMOS transistor comprises a gate, (Ker et al. Figure 9 #50'), for receiving a voltage to turn on the NMOS transistor.

11. Referring to claim 11, an integrated circuit device, wherein the third n-type portion, (Ker et al. Figure 7 #46 & Zhang et al. Figure 2D #111), and the third p-type portion, (Ker et al. Figure 7 #46b & Zhang et al. Figure 2D #112), are contiguous with the isolation layer, (Zhang et al. Figure 2 D #102).

12. Referring to claim 12, an integrated circuit device, wherein the second n-type portion, (Ker et al. Figure 7 #42), includes a fourth p-type portion, (Ker et al. Figure 7 #44b), formed spaced apart from the third p-type portion, (Ker et al. Figure 7 #46b), and wherein the third p-type portion, (Ker et al. Figure 7 #46b), and the fourth p-type portion, (Ker et al. Figure 7 #44b), define a source region and a drain region of a PMOS transistor.

13. Referring to claim 13, an integrated circuit device, wherein the PMOS transistor comprises a gate, (Ker et al. Figure 7 #50), for receiving a voltage to turn on the PMOS.

14. Referring to claim 14, an integrated circuit device, wherein the gate of the PMOS transistor is coupled to the anode of the rectifier, the gate is coupled to the anode via the channel of the transistor to the drain, which is the anode of the circuit.

15. Referring to claim 15, an integrated circuit device, wherein the second p-type portion, (Ker et al. Figure 9 #52), includes a fourth n-type portion, (Ker et al. Figure 9 #46a), formed spaced apart from the first n-type portion, (Ker et al. Figure 9 #46b), and contiguous with the fourth p-type portion, (Ker et al. Figure 7 #44b), and wherein the first n-type portion, (Ker et al. Figure 9 #46b), and the fourth n-type portion, (Ker et al. Figure 9 #46a), define a source region and a drain region of an NMOS transistor.

16. Referring to claim 16, an integrated circuit device, further comprising at least one isolation portion, (Zhang et al. Figure 2 D #102), formed contiguous with the rectifier.

17. Referring to claim 17, an integrated circuit device, comprising: a semiconductor substrate, (Zhang et al. Figure 2D #101); an isolation layer, (Zhang et al. Figure 2 D #102), formed over the semiconductor substrate, (Zhang et al. Figure 2D #101), an n-type MOS transistor having a gate, (Ker et al. Figure 9 #50' & Zhang et al. Figure 2D #109), a drain region, (Ker et al. Figure 9 #46a & Zhang et al. Figure 2D #116), and a source region, (Ker et al. Figure 9 #46b & Zhang et al. Figure 2D #114), formed over the isolation layer, (Zhang et al. Figure 2 D #102); and a p-type MOS transistor having a gate, (Ker et al. Figure 7 #50 & Zhang et al. Figure 2D #107), a drain region, (Ker et al. Figure 7 #44a & Zhang et al. Figure 2D #113), and a source region, (Ker et al. Figure 7 #44b & Zhang et al. Figure 2D #111), formed over the isolation layer, (Zhang et al. Figure 2 D #102), and contiguous with the n-type MOS transistor, wherein the n-

type MOS transistor and the p-type MOS transistor form a rectifier to provide electrostatic discharge protection.

Ker et al. teaches all of the claimed matter in claim 17 except for the rectifier consisting of a CMOS circuit in a detailed Figure but instead teaches it as separate NMOS and PMOS circuitry. Ker et al. does teach the benefits of a CMOS ESD protection circuit in Paragraph 0004. Zhang et al. does teach a CMOS circuit with the source and drain regions of the NMOS and PMOS transistors in a contiguous layout. It would have been obvious to one skilled in the art to combine the teachings of Ker et al. with the teachings of Zhang et al. because the having the source and the drain region contiguously connected reduces the off current and allows the device to be made smaller.

18. Referring to claim 33, a method for protecting a silicon-on-insulator semiconductor, (Zhang et al. Figure 2 D #101 & 102), circuit from electrostatic discharge, comprising: providing an n-type MOS transistor having a source region, (Ker et al. Figure 9 #46b & Zhang et al. Figure 2D #114), and a drain region, (Ker et al. Figure 9 #46a & Zhang et al. Figure 2D #116), in the silicon-on-Insulator, (Zhang et al. Figure 2 D #101 & 102), circuit; providing a p-type MOS transistor having a source region, (Ker et al. Figure 7 #44b & Zhang et al. Figure 2D #111), and a drain region, (Ker et al. Figure 7 #44a & Zhang et al. Figure 2D #113), the p-type MOS transistor being contiguous with the n-type MOS transistor, (Zhang et al. Figure 2D); providing a p-type region, (Ker et al. Figure 9 #44), contiguous with one of the source region and the drain region, (Ker et al. Figure 9 #46b), of the n-type MOS transistor to form a cathode; and providing an n-type region contiguous, (Ker et al. Figure 7 #46), with one of the source region and the drain region, (Ker et al. Figure 7 #44b), of the p-type MOS transistor to form an anode, wherein

the n-type region, the p-type region, the p-type MOS transistor and the n-type MOS transistor form a rectifier.

Ker et al. teaches all of the claimed matter in claim 17 except for the rectifier consisting of a CMOS circuit in a detailed Figure but instead teaches it as separate NMOS and PMOS circuitry. Ker et al. does teach the benefits of a CMOS ESD protection circuit in Paragraph 0004. Zhang et al. does teach a CMOS circuit with the source and drain regions of the NMOS and PMOS transistors in a contiguous layout. It would have been obvious to one skilled in the art to combine the teachings of Ker et al. with the teachings of Zhang et al. because the having the source and the drain region contiguously connected reduces the off current and allows the device to be made smaller.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18-32 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication 2002/0084490 Ker et al., (The English translation of Taiwanese Patent No. 90100080), in view of U.S. Patent No. 5,824,573 Zhang et al. in further view of U.S. Patent No. 5,631,793 Ker et al.

19. Referring to claim 18, an integrated circuit device, further comprising an electrostatic discharge circuit for providing the bias voltage to trigger the rectifier, the electrostatic discharge circuit comprising a first inverter, (Ker et al. (Patent 5,631,793) Figure 2 #223), including a first PMOS transistor having a gate, a source region and a drain region, (Ker et al. (Patent 5,631,793) Figure 2 #Mp1), and a first NMOS transistor having a gate, a source region and a drain region, (Ker et al. (Patent 5,631,793) Figure 2 #Mn1), wherein the gate of the first PMOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mp1), is coupled to the gate of the first NMOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mn1), and the gate of the p-type MOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mp1), is coupled to the drain region of the first PMOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mp1), and the drain region of the first NMOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mn1).

Ker et al. teaches all of the claimed matter except for the rectifier consisting of a CMOS circuit in a detailed Figure but instead teaches it as separate NMOS and PMOS circuitry. Ker et al. does teach the benefits of a CMOS ESD protection circuit in Publication 2002/0084490 Paragraph 0004. Zhang et al. does teach a CMOS circuit with the source and drain regions of the NMOS and PMOS transistors in a contiguous layout. It would have been obvious to one skilled in the art to combine the teachings of Ker et al. with the teachings of Zhang et al. because the having the source and the drain region contiguously connected reduces the off current and allows the device to be made smaller.

20. Referring to claim 19, an integrated circuit device, wherein the gate of the p-type MOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mp1), is coupled to receive the bias voltage to

trigger, (Ker et al. (Patent 5,631,793) Figure 2 #21), the rectifier to provide electrostatic discharge protection, (Ker et al. (Patent 5,631,793) Col. 5 Lines 20-23).

21. Referring to claim 20, an integrated circuit device, wherein the electrostatic discharge circuit further comprises a second inverter, including a second PMOS transistor having a gate, a source region and a drain region, and a second NMOS transistor having a gate, a source region and a drain region, wherein the gate of the second PMOS transistor is coupled to the gate of the second NMOS transistor, and the gate of the n-type MOS transistor is coupled to the drain region of the second PMOS transistor and the drain region of the second NMOS transistor.

Ker et al. discloses the claimed invention except for a second inverter. It would have been obvious to one having ordinary skill in the art at the time the invention was made to add a second inverter for additional buffering, since it has been held that mere duplication of essential working parts of a device involve only routine skill in the art. In re Japikse, 86 USPQ 70

22. Referring to claim 21, an integrated circuit device, wherein the source region of the first NMOS transistor is coupled to ground, (Ker et al. (Patent 5,631,793) Figure 2 Vss).

23. Referring to claim 22, an integrated circuit device, wherein the source region of the second NMOS transistor is coupled to ground.

Ker et al. discloses the claimed invention except for a second inverter. It would have been obvious to one having ordinary skill in the art at the time the invention was made to add a second inverter for additional buffering, since it has been held that mere duplication of essential working parts of a device involve only routine skill in the art. In re Japikse, 86 USPQ 70

24. Referring to claim 23, an integrated circuit device, wherein the source region of the first PMOS transistor is coupled to a pad to receive an electrostatic current, (Ker et al. (Patent 5,631,793) Figure 2 Mp1 & 21).

25. Referring to claim 24, an integrated circuit device, wherein the source region of the second PMOS transistor is coupled to a pad to receive an electrostatic current.

Ker et al. discloses the claimed invention except for a second inverter. It would have been obvious to one having ordinary skill in the art at the time the invention was made to add a second inverter for additional buffering, since it has been held that mere duplication of essential working parts of a device involve only routine skill in the art. In re Japikse, 86 USPQ 70

26. Referring to claim 25, an integrated circuit device, further comprising a first n-type region, wherein one of the source region and the drain region of the p-type MOS transistor, (Ker et al. (Publication 2002/0084490) Figure 9), and the first n-type region form an anode, (Ker et al. (Publication 2002/0084490) Figure 9 #44 & 46b), of the rectifier.

27. Referring to claim 26, an integrated circuit device, further comprising an electrostatic discharge circuit for providing the bias voltage to trigger the rectifier, the electrostatic discharge circuit comprising a first inverter, (Ker et al. (Patent 5,631,793) Figure 2 #223), including a first PMOS transistor having a gate, a source region and a drain region, (Ker et al. (Patent 5,631,793) Figure 2 #Mp1), and a first NMOS transistor having a gate, a source region and a drain region, (Ker et al. (Patent 5,631,793) Figure 2 #Mn1), wherein the gate of the first PMOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mp1), is coupled to the gate of the first NMOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mn1), and the gate of the n-type MOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mn1), is coupled to the drain region of the

first PMOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mp1), and the drain region of the first NMOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mn1).

Ker et al. teaches all of the claimed matter except for the rectifier consisting of a CMOS circuit in a detailed Figure but instead teaches it as separate NMOS and PMOS circuitry. Ker et al. does teach the benefits of a CMOS ESD protection circuit in Publication 2002/0084490 Paragraph 0004. Zhang et al. does teach a CMOS circuit with the source and drain regions of the NMOS and PMOS transistors in a contiguous layout. It would have been obvious to one skilled in the art to combine the teachings of Ker et al. with the teachings of Zhang et al. because the having the source and the drain region contiguously connected reduces the off current and allows the device to be made smaller.

28. Referring to claim 27, an integrated circuit device, wherein the anode of the rectifier, (Ker et al. (Patent 5,631,793) Figure 2 #21), coupled to the gate of the p-type MOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mp1).

29. Referring to claim 28, an integrated circuit device, wherein the gate of the first NMOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mn1), and the gate of the first PMOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mp1), are coupled in parallel to a resistor, (Ker et al. (Patent 5,631,793) Figure 2 #221), and a capacitor, (Ker et al. (Patent 5,631,793) Figure 2 #222).

30. Referring to claim 29, an integrated circuit device, wherein the anode of the rectifier is coupled to a pad, (Ker et al. (Patent 5,631,793) Figure 2 #21), to receive an electrostatic current.

31. Referring to claim 30, an integrated circuit device, further comprising an electrostatic discharge circuit, (Ker et al. (Patent 5,631,793) Figure 2), for providing a bias voltage to trigger,

(Ker et al. (Patent 5,631,793) Figure 2 #21), the rectifier to provide electrostatic discharge protection, wherein the gate of the n-type MOS transistor, (Ker et al. (Patent 5,631,793) Figure 2 #Mn1), is coupled to receive the bias voltage.

32. Referring to claim 31, an integrated circuit device, further comprising a first p-type region, wherein one of the source region and the drain region of the n-type MOS transistor, (Ker et al. (Publication 2002/0084490) Figure 7), and the first p-type region, (Ker et al. (Publication 2002/0084490) Figure 7 #46 &44b), form a cathode of the rectifier.

33. Referring to claim 32, an integrated circuit device, wherein the cathode is coupled to at least one diode, (Ker et al. (Patent 5,631,793) Figure 2 #224), to prevent the rectifier from being triggered in a non-ESD operation.

34. Referring to claim 34, a method, further comprising a step of biasing the p-type MOS transistor to trigger the rectifier, (Figure 2 shows one end of the PMOS connected to VDD and the other via the NMOS to Vss).

35. Referring to claim 35, a method, further comprising a step of biasing the n-type MOS transistor to trigger the rectifier, (Figure 2 shows one end of the NMOS connected to Vss and the other via the PMOS to Vdd).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
December 16, 2002

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